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(54) Peripheral unit interface apparatus enabling hot insertion/removal

Peripherieeinheitsschnittstellenanordnung mit Möglichkeit zur Verbindung unter Spannung

Dispositif d'interface d'une unité périphérique insérable sous tension

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(73) Proprietor: **MITSUBISHI DENKI KABUSHIKI KAISHA**
Tokyo 100 (JP)

(72) Inventor: **Takahashi, Akira,**
c/o Mitsubishi Denki K.K
Tokyo 100 (JP)

(74) Representative: **Pfenning, Meinig & Partner**
Mozartstrasse 17
80336 München (DE)

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- **RESEARCH DISCLOSURE, no. 339, July 1992, EMSWORTH, GB, page 529 XP000316629 "Circuit Card with Contacts of Five Different Lengths for Gradual Current Change when Card is Plugged in or Unplugged"**
- **PATENT ABSTRACTS OF JAPAN vol. 18, no. 484 (P-1798), 8 September 1994 & JP-A-06 161606 (MITSUBISHI ELECTRIC CORP), 10 June 1994,**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates to an interface between a peripheral unit, which is powered by electric current fed from a main unit, and the main unit, and more particularly to an interface circuit which allows connection/ disconnection of the peripheral unit to/from the main unit during the electrical operation of the main unit (i.e. when the main unit is switched on).

2. Description of the Prior Art

[0002] Currently, many combinations exist of a main electronic unit and a peripheral unit which is removably attached to the main unit. One example of such a combination is a computer and an optional card. In this example, the computer is a main unit and the optional card is a peripheral unit.

[0003] Peripheral units include not only those that are easily inserted/removed by a user, such as a PCMCIA card, but also a redundant circuit card for a highly reliable computer system, which is attached/detached only by a maintenance operator. In the former case, insertion or removal of the peripheral unit tends to occur while the main unit is powered on (hereinafter, referred to as "hot line connection/ disconnection" or "hot line insertion/extraction"), due to the fact that ordinary users lack sufficient knowledge about the electronic apparatus. Nevertheless, such an action is naturally not recommendable. On the other hand, the latter often necessitates hot line connection/disconnection in order to avoid taking the system down. Either case requires some countermeasures for avoiding malfunction in the main unit or electrical damage to the main and peripheral unit.

[0004] JP6161606 discloses an interface effective for such hot line insertion/extraction of the peripheral unit to/from the main unit (hereinafter referred to as a prior art system), which is illustrated in Fig. 8.

[0005] In this figure, numeral 2 designates a backboard of a main unit, and numeral 3 designates a substrate which corresponds to a peripheral unit. The backboard 2 (i.e. the main unit) is operated by a power supply voltage V.

[0006] The substrate 3 contains a field-effect transistor (FET) 10 for controlling opening and closing of an electric current feeding path, a buffer resister R3 which ensures steady electric current flow during the OFF state of the FET 10 to prevent a abrupt change in electric current caused by ON/OFF operation of the FET 10, and a delay circuit consisting of resisters R1, R2, and a capacitor C1. The delay circuit is employed for delaying the start of the electrical feed when the substrate 3 is inserted into the backboard 2. After a predetermined delay from the insertion of the substrate 3, which is defined by a time constant of the delay circuit, the base voltage of the FET 10 falls to a potential determined by the dividing resisters R1 and R2 and constant electric current feeding is carried out.

[0007] The substrate 3 also contains a delay inhibiting circuit 18 for prohibiting delay generated by the delay circuit, which comprises a photocoupler (PC1) and a resister R4. When electric current flows into the LED of the photocoupler PC1, the transistor of the photocoupler is turned ON, making the voltage across the capacitor 1 zero, which prohibits the delay generation. During this operation, the resister R4 controls the electric current flowing into the LED.

[0008] During the normal operation, the substrate 3 receives an electrical supply through the FET 10, where the input voltage of the FET 10 is Vi. The symbol Vi is only for convenience, and is in fact substantially equal to the source voltage V. On the other hand, the output voltage of the FET 10 is connected to a predetermined load circuit (not shown), and thus, the substrate 3 functions as a peripheral unit.

[0009] The substrate 3 further includes a connecter for connection with the backboard 2. The connecter has a long terminal set, the pin contact of which is relatively long, and a short terminal. The long terminal set includes source terminals and ground terminals and are connected to the corresponding terminal set of the backboard 2. One end of the short terminal is grounded to a signal ground (SG) terminal of the backboard 2, and the other end is connected to the delay inhibiting circuit 18 of the substrate 3. In this structure, even when only a long terminal set is connected to the backboard 2, the source of the FET 10 (with a voltage Vi) is grounded via the resistors R1, R2 and R4, and is connected to the load circuit via the resistor R3, thereby securing electrical current flow in spite of disconnecting state of the short terminal.

[0010] The action of electrical current supply in such a prior art structure will be described in more detail.

(i) Insertion (Attaching) of the Substrate

[0011] When inserting the substrate 3, the long terminal set is first connected with the corresponding terminal set of the backboard 2 and the ground terminals are connected to the SG terminals of the backboard 2, whereby the voltage Vi becomes equal to the source voltage V. Electric current is supplied to the resistors R1 and R2. However, the FET

10 is not turned ON yet at this stage, because the electric current flows via the resistor R4 into the LED of the photocoupler PC1 in the delay inhibiting circuit 18, which puts the transistor of the PC1 in the ON state, resulting in that the voltage across the capacitor C1 becomes equal and the source gate voltage Vgs of the FET 10 becomes 0.

[0012] The short terminal is connected with the corresponding SG of the backboard 2, and the input to the LED of the PC1 is connected to SG. No electric current flows into the LED and the transistor of the PC1 is turned off. Both ends of the capacitor C1 become open, and the charge by Vi to the capacitor is started. The time constant of the delay circuit at this time is represented as the following equation.

$$C = R1*R2*C1/(R1 + R2) \quad (1)$$

[0013] During this operation, the source gate voltage Vgs of the FET is gradually increased, and when a delay time defined by the order of the time constant has passed, the FET 10 is turned ON. Namely, after a predetermined time from the connection of the short terminal, regular electric supply is started. Generally, electric current flowing through the FET 10 increases as Vgs increases, and therefore, the output voltage of the FET 10 increases with a gentle slope as the time constant becomes larger.

[0014] In this manner, electric feeding can be gradually increased with the hot line insertion of the substrate 3. However, in reality, the increase of the electric feeding can not be uniformly achieved due to the presence of the resistor R3, since the resistor R3 starts feeding electric current to the substrate 3 upon connection of only the long terminal set. The presence of the resistor R3 is rather more important for extraction (detaching) of the substrate 3 than for insertion thereof, as will be described below.

(ii) Extraction of the Substrate

[0015] When the extraction of the substrate 3 is started, the short terminal is first detached from the backboard 2. Namely, the LED of the PC1 is disconnected from SG of the backboard 2, the transistor of the PC1 is turned on, and both ends of the capacitor C1 are short-circuited. The voltage across the capacitor C1 become zero, and Vgs of the FET 10 drops instantly and the transistor is immediately turned off. Thus, among the electric supply paths extending to the substrate 3, the current path from the FET 10 is instantaneously shut off, and only the electric current supply via the resistor R3 remains, which is also finally shut off by the disconnection of the long terminal set.

[0016] During the extraction of the substrate 3, the electric current supply is lowered in the final state through two stages, similar to the insertion operation, but the fluctuation in the electric feeding caused by the ON-OFF operation of the FET 10 is larger than that in the insertion operation. This means that, in such a prior art structure, the resistor R3 functions so as to moderate the abrupt shutoff of electric supply caused when the FET 10 is turned off.

[0017] The above mentioned prior art method, which enables the hot line attaching/detaching of the substrate, was conceived in order to overcome the malfunction of the backboard 2 or other substrates which have already been attached to the backboard 2 caused during the insertion of the substrate. More particularly, when the FET 10 is turned on, a large amount of transient current flows into the substrate 3, which causes a fluctuation of the source voltage V, resulting in the malfunction of the backboard or other substrates. Therefore, the prior art method focusses on the electric feeding action during the insertion of the substrate. The phenomena of the transient current is considered from the following two viewpoints.

(i) Transient Current Peak

[0018] When the peak transient current exceeds the feed capacity of the power source of the backboard 2, the source voltage V drops. The prior art method described above mainly aims at solving this problem. The transient current is caused by rush current to a bypass capacitor on the substrate 3, excessive current dissipated at the activation of a circuit element (e.g. integrated CMOS apparatus) mounted on the substrate 3. Problems arise when the transient current exceeds a normal operation current constantly consumed during the normal operation of the substrate 3, because the source of the backboard 2 has a capacity of feeding at least the normal operation current. Accordingly, this problem is to be overcome by ON/OFF control of the FET 10.

(ii) Derivative (Rate of Change) of Transient Current

[0019] As well as the peak value, the differential value of the transient current must be considered. Even when the peak transient current is within the permissible range, a local and momentary drop of the source voltage is caused by the inductance component of the power supply system of the backboard 2 when an abrupt change occurs in electric current. In the prior art system, since the FET 10 is instantaneously turned off during the extraction of the substrate 3,

the rate of change in the transient current is large in spite of the presence of the buffer resister R3. Also during the insertion of the substrate, the rate of change of the transient current is discontinuous when the FET 10 is turned on, in the case that the circuit constant of, for example, the delay circuit is not carefully selected.

[0020] Thus, when discussing the voltage fluctuation in the backboard 2, not only a peak transient current, but also a rate of change must be considered

[0021] The IBM Technical Disclosure Bulletin (vol.37, No. 09, September 1994 Armonk, NY, pages 315-316) describes a circuit for allowing the installation or remoral of a pluggable device. A MOSFET field effect transistor is controlled so that the voltage on the line rises and falls in a controlled manner, reducing transient conditions. Timing components R2, R5 and C2 assure that MOSFET transistors are turned on in a smooth manner.

[0022] The MOSFET transistors are turned on, after electrical connections are made and a normally-closed switch S1 is opened by plugging the device. The MOSFET transistors are turned off, before electrical connections are broken and when switch S1 is closed by unplugging the device.

3. Summary of the Invention

[0023] In order to overcome the above-mentioned problems (i) and (ii), it is an object of the invention as defined in claim 1 to achieve a smooth increase and decrease of electric current flow both at the time of starting and the time of stopping the electric current feeding from the main electronic unit to the peripheral unit. This should be realized in the form of an interface system between the main and peripheral units, since it is not always possible to provide such a circuit in only one of the main or peripheral units.

[0024] It is another object of the invention to obviate the buffer resistance R3 to reduce the size of the peripheral unit. Generally, the resistance of the resistor R3 must be small in order to give a constant buffer effect, and therefore, the resistor R3 must dissipate a large amount of electric power. This means that the size of a resistor must be large, which is disadvantageous for miniaturization of the peripheral unit due to its large mounting area and unnecessary heat generation. Also, it is necessary to set the resistance value of R3 to a most appropriate one for each peripheral unit in connection with the electric current flowing in response to the ON/OFF operation of the FET 10.

[0025] In order to achieve the objects, an interface system between a peripheral unit and a main unit, in accordance with the invention as defined in claim 1, comprises monitor means for monitoring whether or not the peripheral unit is in a predetermined state where it is completely inserted into (or connected with) the main unit, and control means for controlling electric current supply from the main unit to the peripheral unit. In this structure, the monitor means checks whether or not the connection between the peripheral unit and the main unit is in a predetermined complete state. In parallel to this operation, electric current control means controls the electric current supplied from the main unit to the peripheral unit on the basis of the monitoring result obtained by the monitor means.

[0026] More particularly, during the insertion of the peripheral unit into the main unit, the control means prohibits electric current feeding to the peripheral unit until it has reached the completely inserted state, while, after reaching the completely inserted state, it starts and gradually increases electric current feeding to the peripheral unit for a predetermined time period and then maintains a steady electric current supply.

[0027] During the extraction of the peripheral unit from the main unit, steady electric current supply is maintained before the peripheral unit is taken out of the completely inserted state, while electric current feeding is gradually decreased when the peripheral unit is taken out of the completely inserted state, and is finally stopped after a predetermined time period. As a result, not only the peak value of the transient electric current flowing from the main unit to the peripheral unit, but also the derivative (rate of change) can be maintained within a predetermined range, reducing the possibility of malfunctions in the main or peripheral units caused by fluctuation of the source voltage. Furthermore, as a secondary effect, the buffer resistance required for the conventional method can be obviated, conferring a design advantage.

[0028] The interface system further comprises a connector for connecting the peripheral unit to the main unit. The connector includes long terminal pairs consisting of female pins and long male pins, and at least one short terminal pair consisting of at least one female pin and a short male pin. The state where the short terminal pair is connected is defined as a completely inserted state. By monitoring the connecting state of the short terminal pair between the main unit and peripheral unit, the monitor means can determine whether they are in a completely inserted state. This type of connector is common, and is easily applicable to the present invention.

[0029] The long terminal pairs include at least source terminal pairs for supplying electric current from the main unit to the peripheral unit, and ground terminal pairs. Prior to the complete insertion, the signal ground terminals are first connected while receiving a source voltage from the main unit via the source terminals, preparing for the complete insertion.

[0030] The monitor means includes a signal line indicating the state of electric current flow. The value of electric current flow is varied depending on the connecting state of the peripheral unit to the main unit. The electric current control means includes a delay circuit receiving an input voltage, the value of which is varied depending on the electric

current flowing through the state indicating signal line. By converting the differential of the electric current into a voltage and by delaying it, transient time of the electric current supply can be easily determined.

[0031] The delay circuit may be a integrating circuit including a resistor and a capacitor, and the predetermined time period for the gradual increase and decrease of electric current feeding is determined based on the time constant of the delay circuit. The transient time is also accurately determined based on the time constant.

[0032] During the extraction of the peripheral unit from the main unit, the time constant is set to equal to or smaller than the predetermined time period taken from start to completion of extraction. Thus, the electric current feeding from the main unit will have been stopped by the time of complete extraction, thereby preventing instantaneous cutoff of electric current, and reducing the possibility of fluctuation in the source voltage of the main unit.

[0033] As a further modification, the monitor means includes a state indicating signal line, through which the electric current flows at a value varied depending on the connecting state of the peripheral unit to the main unit, and the electric control circuit includes a signal integrator and a switching element for ON/OFF control of the electric current path from the main unit to the peripheral unit. The output of the signal integrator is connected to the ON/OFF control terminal of the switching element regardless of whether the connection between the main and peripheral units is in the completely inserted state or not.

[0034] In this structure, the input voltage to the signal integrator is varied depending on whether the completely inserted state is achieved or not, which naturally means that the output of this circuit is also varied depending on the connection state of the main and peripheral units. Accordingly, it is possible to separately carry out the ON/OFF control of the switching element between the completely inserted state and the other state. The signals integrated by the integrator show gentle changes, which allows the ON/OFF operation of the switching element to be performed gradually, with a minimum fluctuation in the source voltage of the main unit.

[0035] The electric current control means may further include a second signal integrator, to which a voltage is applied at a value varied in accordance with the electric current value through the state indicating signal line. The output of the second integrator is connected to the ON/OFF control terminal of the switching element only when the connection state between the main and peripheral units is the completely inserted state. When the completely inserted state is achieved, both the first and second signal integrators take part in the ON/OFF control of the switching element. On the other hand, when detaching the peripheral unit (i.e. moving out of the completely inserted state), only the first signal integrator effects the ON/OFF control of the switching element. Thus, it is possible to separately carry out the ON/OFF control of the switching element between the inserting operation and the removing operation. As a result, the time constant for the insertion can be set to be large because the transient electric current is an important problem, while the time constant for the extraction can be set to be small because it is desired to stop the electric current feeding within a predetermined time.

[0036] The output of the second signal integrator is connected to the ON/OFF control terminal through the signal line which forms a closed loop between the main and peripheral units only when the peripheral unit is in the completely inserted state. In this structure, only during the completely inserted state, electric current flows in the closed loop to generate a necessary voltage for controlling the ON/OFF state of the switching element.

[0037] The output of the second signal integrator may be connected to the ON/OFF control terminal via a second switching element which is turned ON only when the peripheral unit is in the completely inserted state. During the completely inserted state, both the first and second signal integrators take part in the ON/OFF control of the switching element, while when not in the completely inserted state, only the first signal integrator effects the ON/OFF control of the switching element. As has been described, it is possible to separately carry out the ON/OFF control of the switching element between the inserting operation and the removing operation, and the time constant for the insertion can be set to be large for overcoming the problem of the transient electric current, while the time constant for the extraction can be set to be small for the stopping of the electric current feeding within a predetermined time. The second switching element can obviate a mutual effect between the circuits for determining the time constants for insertion and extraction of the peripheral unit.

[0038] The switching element may be FET, and the output of the signal integrator is connected to the gate of the FET. The electric current feeding is controlled by the ON/OFF operation of the FET. Since the signals integrated by the signal integrator have gentle changes, the ON/OFF operation is gradually performed, thereby maintaining the voltage drop in front of and beyond the transistor within a constant region during the electric current feeding. Also, with a gradual change of Vgs, fluctuation in the source voltage of the main unit can be prevented.

[0039] The state indicating signal line forms a closed loop only when the completely inserted state is achieved, and direct-current flows in the loop only at this time, which can generate a necessary voltage to control the ON/OFF operation of the switching element.

4. Brief Description of the Drawings

[0040] In the attached drawings:

Fig. 1 is a schematic circuit diagram of an interface apparatus;
Fig. 2 is a schematic circuit diagram of another interface apparatus;
Fig. 3 is a schematic circuit diagram of the interface apparatus in accordance with a first embodiment of the invention;
Fig. 4 is a schematic circuit diagram of the interface apparatus showing a modification of the first embodiment;
Fig. 5 is a schematic circuit diagram of the interface apparatus in accordance with a second embodiment of the invention;
Fig. 6 is a schematic circuit diagram of the interface apparatus in accordance with a third embodiment of the invention;
Fig. 7 is a schematic circuit diagram of the interface apparatus in accordance with a fourth embodiment of the invention; and
Fig. 8 is a schematic circuit diagram of the active attachable/detachable interface apparatus in prior art.

5. Detailed Description of the Preferred Embodiment

[0041] The structure of an interface apparatus is shown in Fig. 1, where the same numerals are assigned to the same elements as those shown in Fig. 8.

[0042] The connecting state of the short terminal pair is important, the state where the short terminals pair is connected is defined as a completely inserted state of the peripheral unit 30 into the main unit 20. Whether the completely inserted state is achieved or not is determined by monitoring electric current flowing in a signal line extending from the source terminal via the R1 and R2 to the short terminal (hereinafter referred to as a state indicating signal line). More particularly, only during the completely inserted state, the state indicating signal line forms a closed loop between the main unit 20 and the peripheral unit 30, into which a direct-current flows.

[0043] The voltage applied to the each element of the delay circuit varies in accordance with the value of the electric current flowing in the signal line. Delay in the delay circuit defines a time period for gradual increasing or decreasing of electric current feeding, and after the time period, steady electric current feeding is started, or the feeding is stopped. A delayed signal is presented between R1 and R2 (i.e. output from the delay circuit) and is input to the gate of the FET 10. In other words, the given time period of delay is the time period required for smooth ON/OFF operation of the FET 10 for avoiding an abrupt change in electric current feeding.

[0044] Electric current flow during the hot attaching/ detaching in accordance with the embodiment will now be described.

[1] Insertion (Attaching) of the Peripheral unit

[0045] The long terminal pairs are first connected, the SG of the peripheral unit 30 is connected to the main unit 20, and Vi becomes equal to the source voltage V. At this time, the state indicating signal line is still open, and no electric current flows. The voltage across the capacitor C1 becomes zero, and the FET 10 is in the OFF state. This structure allows the delay inhibiting circuit 18, which is necessary for the conventional technique, to be obviated.

[0046] The short terminal pair is connected to achieve the completely inserted state, and C1 is charged by Vi. The time constant of the delay circuit at this time is expressed by the equation (1), similarly to the conventional method. The source gate voltage Vgs of the FET 10 becomes higher, and the value of electric current flowing in the transistor gradually increases. Generally, in the FET, the rate of increase of the electric current flow is in proportion to the source gate voltage (i.e. the smaller the Vgs, the smaller the increasing rate). Therefore, the derivative (i.e. rate of change) of the electric current flow is substantially 0 at the start of the electric current feeding. As a result, smooth increasing of electric current feeding is achieved.

[0047] The values of the resistors R1 and R2 are set so as to satisfy the following equation in order to assure that the FET 10 can supply necessary and sufficient electric current for the normal operation.

$$R1*Vi/(R1+R2) \geq Vgs0 \qquad (2)$$

where Vgs0 is a gate source voltage which can allow the FET 10 to supply sufficient normal operation electric current, but is not necessarily so high that the FET 10 is completely turned ON, as is understood from the object of the invention. It is preferable to set Vgs to be slightly lower than the voltage allowing FET 10 to be saturated in order to restrict the peak value of the transient current.

[2] Extraction of the Peripheral unit

[0048] The short terminal pair is first disconnected, and the main and peripheral units get out of the completely inserted state. The state indicating signal line becomes open, and the electric charge stored in C1 is discharged through R1. The time constant of the circuit consisting of C1 and R1 is represented as C1*R1. During the discharge, Vgs is gradually decreased, and the electric current flowing in the FET 10 is also decreased. The value of Vgs finally reaches 0. Thus, smooth decrease of electric current feeding is achieved over the range from the normal operation current to zero, and as a result, the buffer resistance R3 can be obviated.

[0049] It should be understood that it is not preferable for the extraction of the peripheral unit to be completed before the value of electric current supply reaches zero, because the completion of the extraction (i.e. disconnection of the long terminal pairs) causes an instantaneous drop of the electric current supply to zero, which may further cause fluctuations in the source voltage of the main unit.

[0050] For this reason, the time constant C1*R1 is set to be smaller than the necessary time period taken for the complete extraction. Though the necessary time period varies depending on, for example, the fitting length of the terminals, it is normally from several milliseconds to several tens of milliseconds. Accordingly, by setting the time constant C1*R1 to, for example, 10 milliseconds, preferable hot-line detaching can be achieved.

[0051] As has been described, smooth increasing and decreasing of electric current can be achieved by means of a FET 10, and the peak value and the rate of change of the transient current can be restricted within a constant range. This effect further leads to obviation of the buffer resistor which is required in the conventional circuit.

[0052] Although the FET is used for opening and closing of the electric current path, other elements such as an ordinary bipolar transistor may be used. However, in the case that voltage drop by the transistor may be a problem, an FET may often be advantageous. Also, in the embodiment, the RC integrator is used as a delay circuit, but it may include any other circuit element, such as an inductance element, as long as the circuit has a delay function and an integral function.

[0053] Fig. 2 shows another interface apparatus circuit. The same numerals are assigned to the same elements as those shown in Fig. 1 and Fig.8.

[0054] The feature of the interface apparatus shown in Fig. 2 is a movable element (not shown) for reinforcing fixing of the peripheral unit to the main unit. The interface apparatus shown in Fig.2 achieves the same effect as the interface apparatus shown in Fig.1. The movable element is a lever which moves between a first position for securing the connection between the main unit and peripheral units and a second position for releasing the securing. The lever is manually operated to select the necessary position.

[0055] The completely inserted state is defined as a state where the lever is in the first position. In reality, there may occur a case that the lever is moved to the first position even when the peripheral units is not inserted. However, this does not cause a problem because the lever is inevitably returned to the second position before the insertion, otherwise insertion will not be allowed.

[0056] This interface apparatus circuit requires a switch SW1 interlock with the lever, as is shown in Fig. 2. The state of the interlock switch is changed in response to the position of the lever. For instance, the switch is adapted to be pushed only when the lever is in the first position. In this structure, it is determined that the peripheral unit is in the completely inserted state only when the switch is pushed down. By monitoring the state of the switch, electric current flow is preferably controlled. In this structure, the path from the source terminal through R1 and R2 to the switch SW1 is a state indicating signal line. Monitoring the state of the switch corresponds to monitoring of the connecting state of the short terminal pair in the first embodiment. Therefore, in this interface apparatus circuit, the contact lengths of the terminal pairs of the connector may all be the same.

[0057] The hot-line attaching and detaching will now be described, emphasizing differences from the interface apparatus circuit, shown in Fig. 1.

[1] Insertion (Attaching) of the Peripheral unit

[0058] As a premise for insertion, the lever must be in the second position, and the switch SW1 in the OFF state. In the insertion, all the terminals are connected at the same time, but the state indicating signal line is still opened.

[0059] The lever is moved to the first position to secure the connection of the main and peripheral units. The SW1 is turned on and charging of the Cl is started. Later operation of electric current feeding is the same as in the interface apparatus circuit, shown in Fig. 1.

[2] Extraction (Detaching) of the Peripheral unit

[0060] Prior to removing the peripheral unit, the lever is returned to the second position from the first position. The main and peripheral units are taken out of the completely inserted state despite that the terminal pairs are still connected,

and the state indicating signal line becomes opened. The C1 starts to be discharged and electric current feeding is stopped within a predetermined time period, similar to the interface apparatus circuit, shown in Fig.1.

[0061] When setting the time constant C1*R1 to be smaller than the required time period taken from starting to finishing extraction, the value of C1*R1 can be set larger than that in the interface apparatus circuit, shown in Fig.1, because the time period for the complete extraction includes extra time for lever operation, normally about 1 second. Therefore, the value of the C1*R1 can be set to, for example, 100 milliseconds. The larger the value of C1*R1, the smaller the rate of change of electric current feeding, which is preferable for circuit design.

[0062] Although in this interface apparatus circuit a lever is used as a movable element, alternatives such as a push-in button or screw can be used. Although the lever is used only for securing and releasing the connection, another type of lever, for example, a type where the lever operation causes the peripheral unit automatically to be pushed out, can be employed. Similarly, various types of interlock switch (e.g. push type, slide type, optical type, etc.) can be used. It is assumed that the switch is turned on when it is pushed down, but of course the reverse is also permissible. In the reverse case, the push-down of the switch is released only when the lever is in the first position.

[0063] The essential feature of a first embodiment, according to the invention, is that a second delay circuit is included, as is seen from Fig. 3. During the insertion, both delay circuits generate delays, while during the extraction, only the first delay circuit generates a delay. This structure is especially effective when a larger delay is required for the insertion operation, while the delay for the extraction operation must be restrained within a desired range.

[0064] The connector includes both long and short terminal pairs, similarly to the interface apparatus circuit, shown in Fig. 1. However, in this embodiment, at least three short terminal pairs "a", "b", and "c" are required. The short terminal pair "a" is used for the same purpose as in the interface apparatus circuit, shown in Fig. 1. The short terminal pairs "b" and "c" are interconnected at the main unit side, and are used as a signal line forming a closed loop between the main and peripheral units during the completely inserted state. This signal line is referred to as a second state indicating signal line.

[0065] The second delay circuit comprises a capacitor C2, a resistor R5, and the resistor R2 shared by the first delay circuit. The capacitor C2 and resistor R5 are arranged in parallel, and are connected between the source terminals (long terminals) and the short terminal "c". The resistor R2 is connected to the short terminal "b".

[0066] In this structure, the first signal line extends from the source terminals via the R1 and R2 to the short terminal "a" (SG), and the second signal line extends in the order of the source terminals - R5 → short terminal "c" - short terminal "b" → R2 → short terminal "a" (SG). Both state indicating signal lines form closed loops only when the short terminal pairs are connected. In the completely inserted state, a delay signal delayed by the second delay circuit is present between R5 and R2, and is referred to as an output signal of the second delay circuit. Differing from the output from the first delay circuit, the output of the second delay circuit is connected to the gate of the FET 10 only in the completely inserted state.

[0067] Electric current feeding for the hot-line attaching/detaching is as follows.

[1] Insertion of the Peripheral unit

[0068] The long terminal pairs are first connected, but no electric feeding is started yet. At least three short terminal pairs are connected, the first and second signal lines form closed loops, respectively, and the capacitors C1 and C2 are charged. The time constant, taking into account the effect of both delay circuits, is expressed as follows.

$$C = R1*R2*R5*(C1+C2)/(R1*R2 + R2*R5 + R5*R1) \quad (3)$$

[0069] The resistance value is set within the range represented as below.

$$Vi*(R1*R2 + R2*R5)/(R1*R2 + R2*R5 + R5*R1) \geq Vgs0 \quad (4)$$

where the definition of Vgs0 is the same as the first embodiment.

[2] Extraction of the Peripheral unit

[0070] When the short terminal pairs are first disconnected, the capacitor C2 and resistor R5 are completely removed from the system of the peripheral unit, and do not take part in the later electric current feeding. Thus, the later behavior of the electric feeding is the same as of the interface apparatus circuit, shown in Fig. 2. The time period taken for complete extraction is provided by the time constant C1*R1.

[0071] In order to set the time constant for insertion to be large, the value of C2 is set large, in reference to the above

equation (3). Since C2 does not effect the time constant for the extraction of the-peripheral unit, the value of C1*R1 can be set small, for example, in the order of 10 milliseconds, thereby realizing relatively quick stopping of electric current feeding before the complete extraction.

[0072] In this embodiment, the monitoring of the completely inserted state of the short terminal pairs can be replaced by the monitoring of the position of the movable element, as is shown in Fig. 4. In such a case, the switch 1 simultaneously controls opening and closing of the first and second signal lines.

[0073] The interface apparatus in accordance with the second embodiment also includes the second delay circuit, but is characterized in that the number of short terminal pairs is reduced to only one and instead, a second FET 12 is provided. This structure is shown in Fig. 5. Disconnection of the second delay circuit during the extraction of the peripheral unit is done by the second FET 12, not by the short terminal pairs. The second FET 12 is provided between the output of the second delay circuit and the base of the FET 10. The gate of the second FET 12 is connected to the short terminal and the signal from the FET 12 is pulled up via the resistor R6 to the source terminal (long terminal). As a result, the second FET 12 can be quickly turned on when the peripheral unit is inserted, and can be quickly turned off when the peripheral electronic device is removed. The second FET 12 is in the ON state only in the completely inserted state.

[0074] The first state indicating signal line extends from the source terminal through R1, the source and drain of the second FET 12, and R2 to the short terminal (SG), while the second signal line extends from the source terminal through R5 and R2 to the short terminal (SG).

[0075] Electric current feeding during the hot-line attaching/ detaching in this embodiment is substantially the same as that in the first embodiment as long as quick ON/OFF operation of the second FET 12 is ensured. Of course, it is possible to substitute the monitoring of the movable element for monitoring of the short terminal.

[0076] Fig. 6 shows an interface apparatus in accordance with the third embodiment of the invention. This embodiment is to completely cut off the second delay circuit, which has not been achieved in the second embodiment. The second delay circuit was cut off by the second FET in the circuit of the second embodiment, differing from the first embodiment in which the cut-off was taken place by extraction of the short terminal. However, in contrast to the fact that the second delay circuit is completely cut off from the system of the peripheral unit 30 when the short terminal is disconnected in the first embodiment, a loop circuit, specifically, the second delay circuit -> R2 -> R6 -> the second delay circuit, remains in the second embodiment. Therefore, a loop circuit, 2nd delay circuit -> R2 -> R6 -> 2nd delay circuit, still remains even after OFF operation of the second FET, which is contrary to the first embodiment where the second delay circuit was completely cut off from the system of the peripheral unit 30 by disconnection of the short terminal. In order to compensate for the incomplete cutting off, in the second embodiment, each of the circuit constants had to be provided by a relatively complex calculation to accurately determine a time constant for the hot line attachment/detachment.

[0077] In the third embodiment, a third FET 14 is provided between the second delay circuit and R2 to cut off the remaining loop circuit, in the third embodiment. The base of the third FET 14 is directly connected to the base of the second FET 12.

[0078] In this structure, the state indicating signal lines are the same as those in the second embodiment, but the second signal line is defined as a line from source terminal → R5 source and drain of 3rd FET → R2 → short terminal (SG).

[0079] It should be understood that the condition of electric current feeding in this embodiment is also the same as that of the first embodiment as long as quick ON/OFF operation of the second and third FETs 12 and 14 is ensured during insertion and extraction of the peripheral unit 30. Instead of monitoring the short terminal, a movable element may be provided, the position of which is monitored to detect the completely inserted state.

[0080] Fig. 7 shows an interface circuit in accordance with the fourth embodiment. The feature of this embodiment is that the time constant for insertion of the peripheral unit 30 is set to be large. This is achieved by connecting the output of the second delay circuit to the gate of the second FET 12, not to the FET 10, to confer a delay to the ON operation of the second FET 12. The second delay circuit does not influence extraction of the peripheral unit 30.

[0081] The second delay circuit consists of a capacitor C2, a resistor R5, and a resistor R7, in which outputs from R5 and R7 are connected to the gate of the second FET 12.

[0082] Electric current feeding for the hot line attaching/detaching is as follows.

[1] Insertion of the Peripheral Unit

[0083] When the peripheral unit is in the completely inserted state where both long and short terminal pairs are connected, electric current flows through R5 and R7 In the second delay circuit to charge the capacitor C2, and the gate voltage of the second FET 12 gradually decreases. The second FET 12 starts to smoothly flow electric current to charge the capacitor C1, and the FET 10 is turned ON. The time constant τ is a large value because it is approximately the sum of the time constant $\tau 1$ of the first delay circuit and the time constant $\tau 2$ of the second delay circuit.

[2] Extraction of the Peripheral Unit

[0084] When the short terminal pair is disconnected, the drain of the second FET 12 is in the state almost equal to the open state, and the second delay circuit is isolated. The time constant for the extraction is represented as C1*R1.

[0085] In this structure, abrupt transition of electric current feeding can be further restricted during insertion of the peripheral unit. This embodiment is more advantageous than the first embodiment, in that it does not need a large value of capacitance for each capacitor. In the first embodiment, a capacitor having a large capacitance was used for C2 for the purpose of increasing the time constant for insertion, while maintaining the time constant for extraction. The size of the capacitor tends to be in proportion to the capacitance thereof, the fourth embodiment is superior to the first one.

[0086] Although, in the above-described embodiments, the power source applies positive voltage to the apparatus, negative voltage is also applicable.

Claims

1. An interface apparatus for connecting through insertion/extraction, a peripheral unit (30) to and from a main unit (20) during electrical operation of the main unit (20), the peripheral unit (30) being powered by electric current fed from the main unit (20) through the interface apparatus, comprising:

   monitor means for monitoring whether or not the peripheral unit (30) is in a predetermined completely inserted state to the main unit (20); and
   control means for controlling electric current supply from the main unit (20) to the peripheral unit (30), said control unit, for the insertion, prohibiting electric current supply before the peripheral unit (30) reaches the completely inserted state, starting and gradually increasing electric current supply during a first predetermined time period after the peripheral unit (30) reaches the completely inserted state, and maintaining steady electric current supply after the first predetermined time period, while, for the extraction of the peripheral unit (30), said control unit maintaining the steady electric current supply until the peripheral unit (30) is out of the completely inserted state,

   characterized by

   gradually decreasing electric current supply during a second predetermined time period after the peripheral unit (30) is out of the completely inserted state, and stopping the electric current supply after the second predetermined time period,
   wherein the first predetermined time period is defined by delays generated by a first (C1, R1) and a second (C2, R5) delay circuit and the second predetermined time period is defined by a delay generated solely by the first delay circuit (C1, R1).

2. The interface apparatus according to claim 1, further comprising a connector for connecting the peripheral unit (30) and the main unit (20), said connector including long terminal pairs having a long pin contact and at least one short terminal pair having a short contact length, wherein said completely inserted state is defined as a state where the short terminal pair is connected, and said monitor means monitors the connecting state of the short terminal pair to determine whether or not the peripheral unit (30) is in the completely inserted state.

3. The interface apparatus according to claim 2, wherein the long terminal pairs include at least source terminal pairs for supplying electric current from the main unit (20) to the peripheral unit (30), and grounding terminal pairs.

4. The interface apparatus according to claim 1, wherein said monitor means includes a state indicating signal line, through which electric current flows with the value being varied depending on whether the peripheral unit (30) is in the completely inserted state or not, wherein the first delay circuit (C1, R1) is coupled to the state indicating signal line to receive a different voltage in accordance with the amount of electric current value flowing in the state indicating signal line.

5. The interface apparatus according to claim 4, wherein the first delay circuit is an integrator including a resistor (R1) and a capacitor (C1), and the first predetermined time period is defined on the basis of a time constant of the delay circuit.

6. The interface apparatus according to claim 5, wherein the second predetermined time period is set to be smaller than a time period taken from starting to completion of the extraction of the peripheral unit (30).

7. The interface apparatus according to claim 1, wherein said monitor means includes a state indicating signal line, through which electric current flows with the value being varied depending on whether the peripheral unit (30) is in the completely inserted state or not, wherein the first delay circuit (C1, R1) includes an integrator, to which a different voltage is applied in accordance with the electric current value, and the control means includes a first switching element (10) for controlling opening and closing of an electric current path supplied from the main unit (20) to the peripheral unit (30), the output of the integrator (C1, R1) being connected to the opening/closing control terminal of the first switching element (10) irrespective of whether the peripheral unit (30) is in the completely inserted state or not.

8. The interface apparatus according to claim 7, wherein the second delay circuit (C2, R5) includes a second integrator, to which a different voltage is applied in accordance with the value of the electric current flowing through the state indicating signal line, the output of the second integrator (C2, R5) being connected to the opening/closing control terminal of the first switching element (10) only when the peripheral unit (30) is in the completely inserted state.

9. The interface apparatus according to claim 8, wherein said output of the second integrator (C2, R5) is connected to the opening/closing control terminal of the first switching element (10) via a signal line which forms a closed loop only when the peripheral unit (30) is in the completely inserted state.

10. The interface apparatus according to claim 8, wherein said control means further includes a second switching element (12), and the output of the second integrator (C2, R5) is connected via the second switching element (12) to the opening/closing control terminal of the first switching element (10).

11. The interface apparatus according to claim 7, wherein the first switching element (10) is a FET, and the output of the first integrator (C1, R1) is connected to the gate of the FET.

12. The interface apparatus according to claim 7, wherein said state indicating signal line forms a closed loop only when the peripheral unit (30) is in the completely inserted state, and only at that time, does direct electric current flow in the state indicating signal line.

Patentansprüche

1. Schnittstellenanordnung zum Verbinden einer peripheren Einheit (30) mit und von einer Haupteinheit (20) durch Einführen/Herausziehen während des elektrischen Betriebs der Haupteinheit (20), wobei die periphere Einheit (30) gespeist wird durch einen elektrischen Strom, der von der Haupteinheit (20) durch die Schnittstellenanordnung zugeführt wird, welche aufweist:

   Überwachungsmittel, welche überwachen, ob die periphere Einheit (30) in einem vorbestimmten vollständig eingeführten Zustand zu der Haupteinheit (20) ist; und
   Steuermittel zum Steuern der elektrischen Stromzuführung von der Haupteinheit (20) zu der peripheren Einheit (30), wobei die Steuereinheit für die Einführung eine Zuführung des elektrischen Stroms unterbindet, bevor die periphere Einheit (30) den vollständig eingeführten Zustand erreicht, startet und die Zuführung des elektrischen Strom allmählich steigert während einer ersten vorbestimmten Zeitperiode, nachdem die periphere Einheit (30) den vollständig eingeführten Zustand erreicht hat, und Aufrechterhalten einer ständigen elektrischen Stromzuführung nach der ersten vorbestimmten Zeitperiode, während für das Herausziehen der peripheren Einheit (30) die Steuereinheit die ständige elektrische Stromzuführung aufrecht erhält, bis die periphere Einheit (30) aus dem vollständig eingeführten Zustand heraus ist,

   gekennzeichnet durch
   allmähliche Abnahme der elektrischen Stromzuführung während einer zweiten vorbestimmten Zeitperiode, nachdem die periphere Einheit (30) aus dem vollständig eingeführten Zustand heraus ist, und Anhalten der elektrischen Stromzuführung nach der zweiten vorbestimmten Zeitperiode, worin die erste vorbestimmte Zeitperiode definiert ist durch von einer ersten (C1, R1) und einer zweiten (C2, R5) Verzögerungsschaltung erzeugte Verzögerungen und die zweite vorbestimmte Zeitperiode definiert ist durch eine nur von der ersten Verzögerungsschaltung (C1,

R1) erzeugte Verzögerung.

2. Schnittstellenanordnung nach Anspruch 1, weiterhin aufweisend einen Verbinder zum Verbinden der peripheren Einheit (30) und der Haupteinheit (20), wobei der Verbinder ein langes Anschlußpaar mit einem langen Stiftkontakt und zumindest ein kurzes Anschlußpaar mit einer kurzen Kontaktlänge enthält, worin der vollständig eingeführte Zustand definiert ist als ein Zustand, in welchem das kurze Anschlußpaar verbunden ist, und die Überwachungsmittel den Verbindungszustand des kürzen Anschlußpaares überwachen, um zu bestimmen, ob die periphere Einheit (30) in dem vollständig eingeführten Zustand ist oder nicht.

3. Schnittstellenanordnung nach Anspruch 2, worin die langen Anschlußpaare zumindest Quellenanschlußpaare enthalten zum Zuführen eines elektrischen Stroms von der Haupteinheit (20) zu der peripheren Einheit (30) und zum Erden von Anschlußpaaren.

4. Schnittstellenanordnung nach Anspruch 1, worin die Überwachungsmittel eine Zustandsanzeige-Signalleitung enthalten, durch welche ein elektrischer Strom fließt mit einem Wert, der abhängig davon verändert wird, ob die periphere Einheit (30) in dem vollständig eingeführten Zustand ist oder nicht, worin die erste Verzögerungsschaltung (C1, R1) mit der Zustandsanzeige-Signalleitung gekoppelt ist, um eine unterschiedliche Spannung zu empfangen gemäß der Größe des Wertes des elektrischen Stroms, der in der Zustandsanzeige-Signalleitung fließt.

5. Schnittstellenanordnung nach Anspruch 4, worin die erste Verzögerungsschaltung ein Integrator ist, der einen Widerstand (R1) und einen Kondensator (C1) enthält, und die erste vorbestimmte Zeitperiode definiert ist auf der Grundlage einer Zeitkonstanten der Verzögerungsschaltung.

6. Schnittstellenanordnung nach Anspruch 5, worin die zweite vorbestimmte Zeitperiode so eingestellt ist, daß sie kleiner ist als eine Zeitperiode von dem Beginn bis zur Beendigung des Herausziehens der peripheren Einheit (30).

7. Schnittstellenanordnung nach Anspruch 1, worin die Überwachungsmittel eine Zustandsanzeige-Signalleitung enthalten, durch welche ein elektrischer Strom fließt, dessen Wert in Abhängigkeit davon verändert wird, ob die periphere Einheit (30) in dem vollständig eingeführten Zustand ist oder nicht, worin die erste Verzögerungsschaltung (C1, R1) einen Integrator enthält, an welchen eine unterschiedliche Spannung angelegt wird gemäß dem Wert des elektrischen Stroms, und die Steuermittel ein erstes Schaltelement (10) enthalten zum Steuern des Öffnens und Schließens eines Pfades für den elektrischen Strom, der von der Haupteinheit (20) zu der peripheren Einheit (30) geliefert wird, und der Ausgang des Integrators (C1, R1) mit dem Öffnungs/Schließ-Steueranschluß des ersten Schaltelements (10) verbunden ist ungeachtet dessen, ob die periphere Einheit (30) in dem vollständig eingeführten Zustand ist oder nicht.

8. Schnittstellenanordnung nach Anspruch 7, worin die zweite Verzögerungsschaltung (C2, R5) einen zweiten Integrator enthält, an welchen eine unterschiedliche Spannung angelegt wird gemäß dem Wert des elektrischen Stroms, der durch die Zustandsanzeige-Signalleitung fließt, wobei der Ausgang des zweiten Integrators (C2, R5) mit dem Öffnungs/Schließ-Steueranschluß des ersten Schaltelements (10) nur verbunden ist, wenn die periphere Einheit (30) in dem vollständig eingeführten Zustand ist.

9. Schnittstellenanordnung nach Anspruch 8, worin der Ausgang des zweiten Integrators (C2, R5) mit -dem Öffnungs/Schließ-Steueranschluß des ersten Schaltelements (10) über eine Signalleitung verbunden ist, welche nur dann eine geschlossene Schleife bildet, wenn die periphere Einheit (30) in dem vollständig eingeführten Zustand ist.

10. Schnittstellenanordnung nach Anspruch 8, worin die Steuermittel weiterhin ein zweites Schaltelement (12) enthalten und der Ausgang des zweiten Integrators (C2, R5) über das zweite Schaltelement (12) mit dem Öffnungs/Schließ-Steueranschluß des ersten Schaltelements (10) verbunden ist.

11. Schnittstellenanordnung nach Anspruch 7, worin das erste Schaltelement (10) ein FET ist und der Ausgang des ersten Integrators (C1, R1) mit dem Gate des FET verbunden ist.

12. Schnittstellenanordnung nach Anspruch 7, worin die Zustandsanzeige-Signalleitung nur dann eine geschlossene Schleife bildet, wenn die periphere Einheit (30) in dem vollständig eingeführten Zustand ist, und nur zu dieser Zeit fließt ein elektrischer Gleichstrom in der Zustandsanzeige-Signalleitung.

Revendications

1. Dispositif d'interface pour, grâce à une opération d'insertion/extraction, connecter à une unité centrale (20) et déconnecter de cette unité centrale une unité périphérique (30) pendant le fonctionnement électrique de l'unité centrale (20), l'unité périphérique (30) étant alimentée par un courant électrique fourni par l'unité centrale (20) à travers le dispositif d'interface, comprenant: des moyens de surveillance pour surveiller si l'unité périphérique (30) est dans un état prédéterminé de complète insertion ou non par rapport à l'unité centrale (20) ; et des moyens de commande pour commander l'alimentation en courant électrique de l'unité centrale (20) vers l'unité périphérique (30), ladite unité de commande empêchant, pour l'insertion, l'alimentation en courant électrique avant que l'unité périphérique (30) n'atteigne l'état de complète insertion, amorçant et augmentant progressivement l'alimentation en courant électrique pendant une première période temporelle prédéterminée après que l'unité périphérique (30) ait atteint l'état de complète insertion, et maintenant l'alimentation en courant électrique constante après la première période temporelle prédéterminée, tandis que, pour l'extraction de l'unité périphérique (30), ladite unité de commande maintient l'alimentation en courant électrique constante jusqu'à ce que l'unité périphérique (30) quitte l'état de complète insertion, caractérisé par la diminution progressive de l'alimentation en courant électrique pendant une seconde période temporelle prédéterminée après que l'unité périphérique (30) ait quitté l'état de complète insertion, et l'arrêt de l'alimentation en courant électrique après la seconde période temporelle prédéterminée, dans lequel la première période temporelle prédéterminée est définie par des retards générés par un premier (C1, R1) et un second (C2, R5) circuits à retard et la seconde période temporelle prédéterminée est définie par un retard généré uniquement par le premier circuit à retard (C1, R1).

2. Dispositif d'interface selon la revendication 1, comprenant en outre un connecteur pour connecter l'unité périphérique (30) et l'unité centrale (20), ledit connecteur comprenant des paires de bornes longues ayant un contact de broche long et au moins une paire de bornes courtes ayant une longueur de contact courte, dans lequel ledit état de complète insertion est défini comme un état dans lequel la paire de bornes courtes est connectée, et lesdits moyens de surveillance surveillent l'état de connexion de la paire de bornes courtes afin de déterminer si l'unité périphérique (30) se trouve en état de complète insertion ou non.

3. Dispositif d'interface selon la revendication 2, dans lequel les paires de bornes longues comprennent au moins une paire de bornes d'alimentation afin d'amener le courant électrique de l'unité centrale (20) à l'unité périphérique (30), et des paires de bornes de mise à la masse.

4. Dispositif d'interface selon la revendication 1, dans lequel lesdits moyens de surveillance comprennent une ligne de signaux d'indication d'état, par laquelle le courant électrique circule avec sa valeur qui varie suivant si l'unité périphérique (30) est dans l'état de complète insertion ou non, dans lequel le premier circuit à retard (C1, R1) est couplé à la ligne de signaux d'indication d'état afin de recevoir une tension différente en fonction de la grandeur de la valeur du courant électrique circulant dans la ligne de signaux d'indication d'état.

5. Dispositif d'interface selon la revendication 4, dans lequel le premier circuit à retard est un intégrateur comprenant une résistance (R1) et un condensateur (C1), et la première période temporelle prédéterminée est définie sur la base d'une constante de temps du circuit à retard.

6. Dispositif d'interface selon la revendication 5, dans lequel la seconde période temporelle prédéterminée est fixée comme étant inférieure à une période temporelle comprise entre le début et la fin de l'extraction de l'unité périphérique (30).

7. Dispositif d'interface selon la revendication 1, dans lequel lesdits moyens de surveillance comprennent une ligne de signaux d'indication d'état, par laquelle un courant électrique circule avec sa valeur qui varie suivant si l'unité périphérique (30) est dans l'état de complète insertion ou non, dans lequel le premier circuit à retard (C1, R1) comprend un intégrateur, auquel une tension différente est appliquée en fonction de la valeur du courant électrique, et les moyens de commande comprennent un premier élément de commutation (10) servant à commander l'ouverture et la fermeture d'un trajet de courant électrique fourni par l'unité centrale (20) à l'unité périphérique (30), la sortie de l'intégrateur (C1, R1) étant connectée à la borne de commande d'ouverture/de fermeture du premier élément de commutation (10) sans tenir compte du fait que l'unité périphérique (30) est dans l'état de complète insertion ou non.

8. Dispositif d'interface selon la revendication 7, dans lequel le second circuit à retard (C2, R5) comprend un second intégrateur, auquel est appliquée une tension différente en fonction de la valeur du courant électrique circulant à

travers la ligne de signaux d'indication d'état, la sortie du second intégrateur (C2, R5) étant connectée à la borne de commande d'ouverture/de fermeture du premier élément de commutation (10) seulement quand l'unité périphérique (30) est dans l'état de complète insertion.

9. Dispositif d'interface selon la revendication 8, dans lequel ladite sortie du second intégrateur (C2, R5) est connectée à la borne de commande d'ouverture/de fermeture du premier élément de commutation (10) par l'intermédiaire d'une ligne de signaux qui forme une boucle fermée seulement quand l'unité périphérique (30) est dans l'état de complète insertion.

10. Dispositif d'interface selon la revendication 8, dans lequel lesdits moyens de commande comprennent en outre un second élément de commutation (12), et la sortie du second intégrateur (C2, R5) est connectée par l'intermédiaire du second élément de commutation (12) à la borne de commande d'ouverture/de fermeture du premier élément de commutation (10).

11. Dispositif d'interface selon la revendication 7, dans lequel le premier élément de commutation (10) est un transistor à effet de champ, et la sortie du premier intégrateur (C1, R1) est connectée à la grille du transistor à effet de champ.

12. Dispositif d'interface selon la revendication 7, dans lequel ladite ligne de signaux d'indication d'état forme une boucle fermée seulement quand l'unité périphérique (30) est dans l'état de complète insertion, et seulement à ce moment là, un courant électrique direct circule dans la ligne de signaux d'indication d'état.

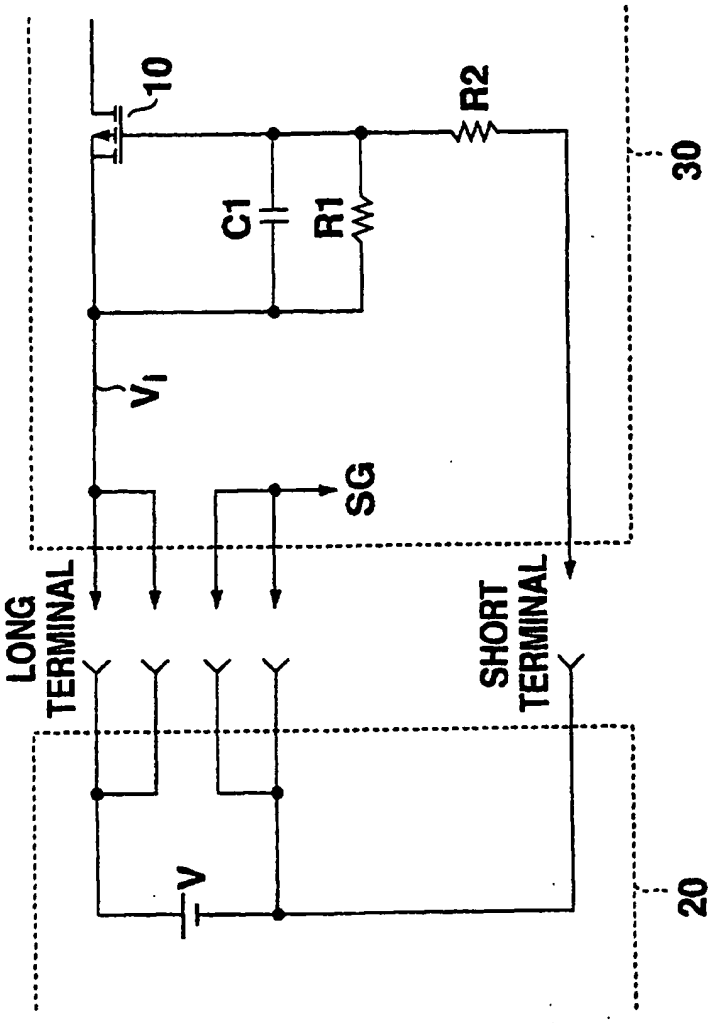

Fig. 1

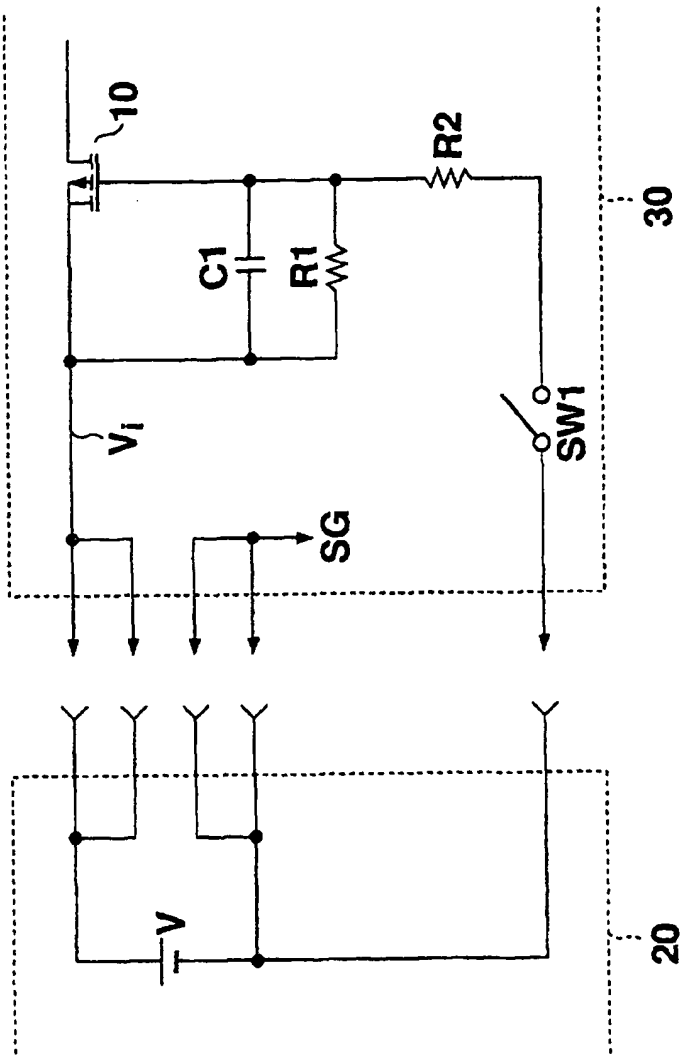

Fig. 2

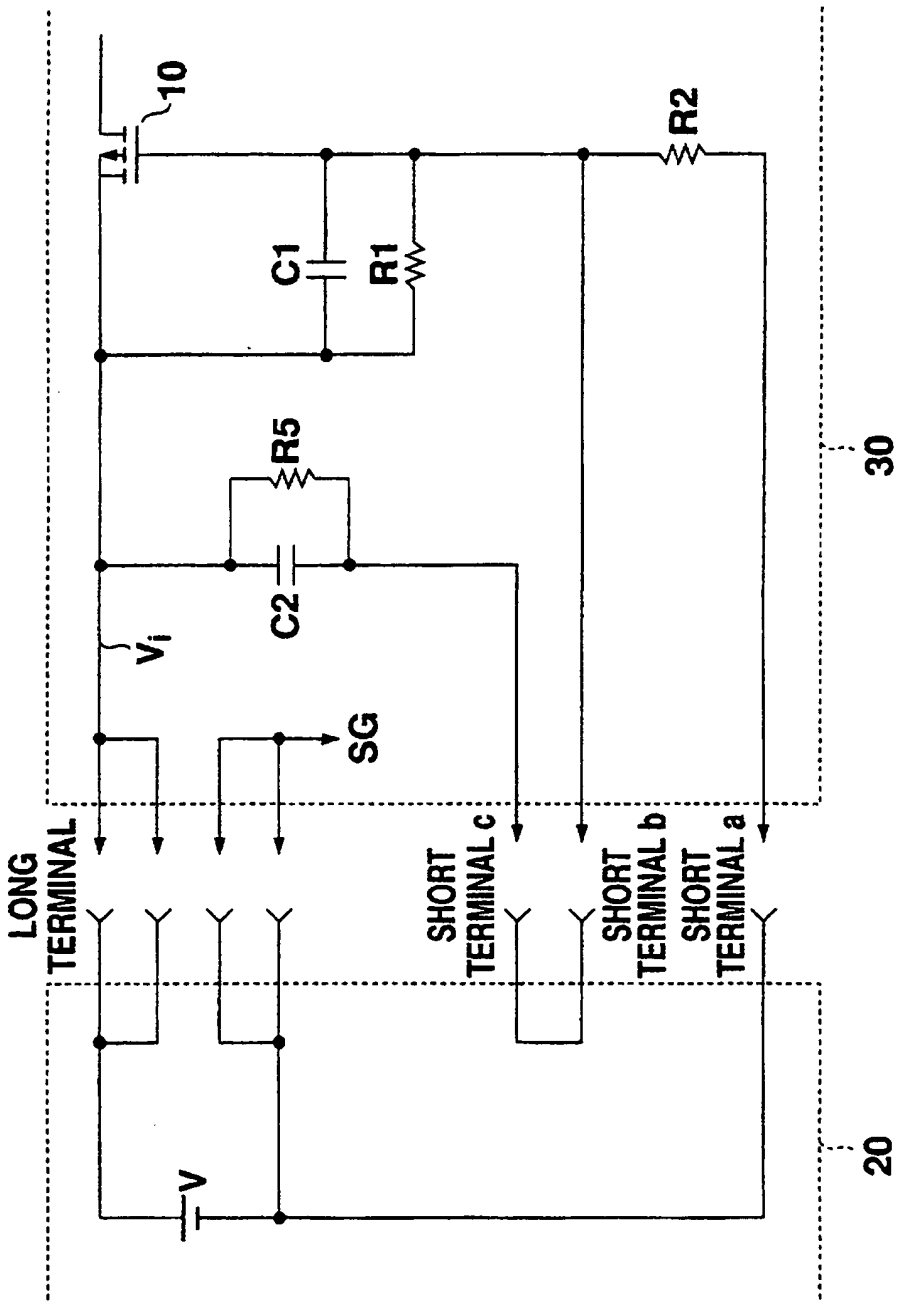
10
R2
C1
R1
R5
C2
V_i
SG
LONG TERMINAL
SHORT TERMINAL c
SHORT TERMINAL b
SHORT TERMINAL a
30
20
V

Fig. 3

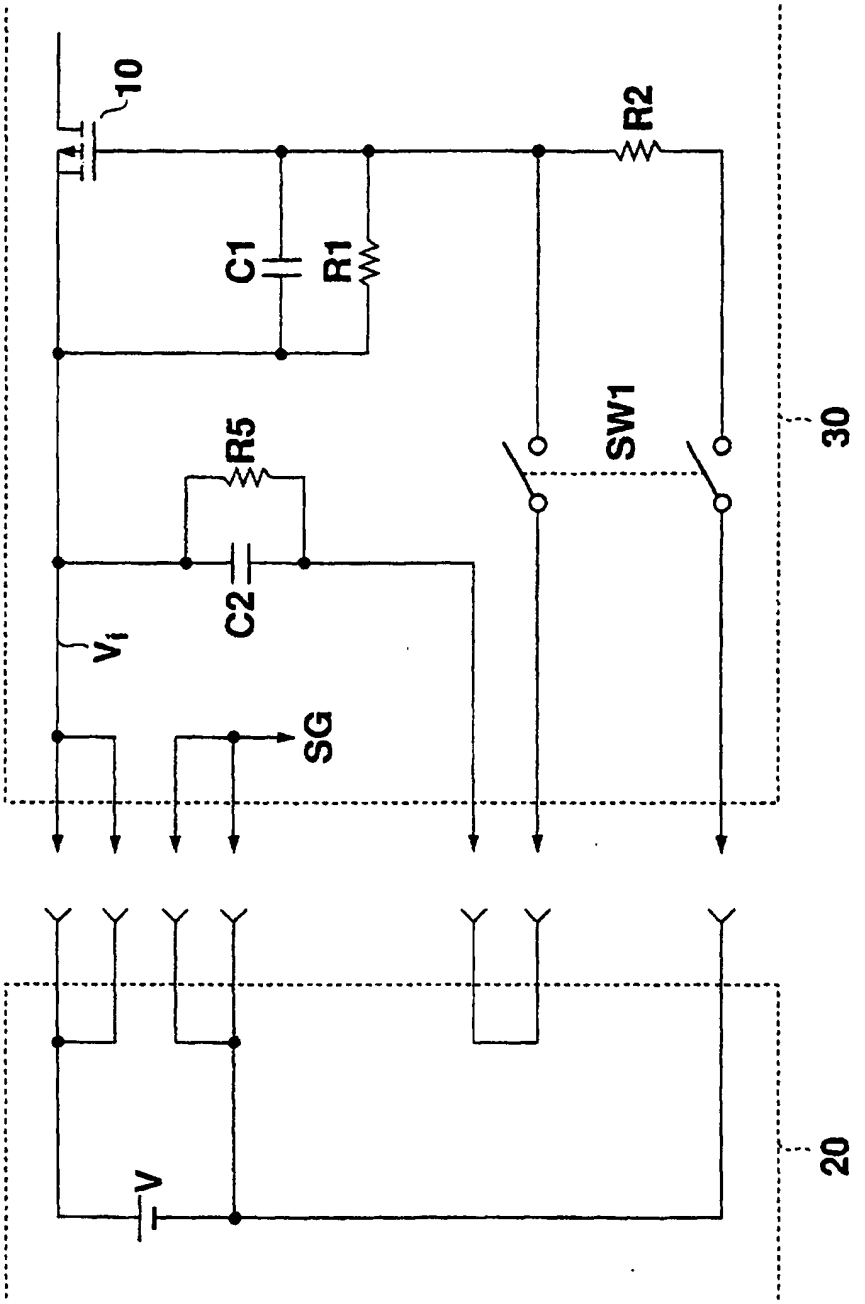

Fig. 4

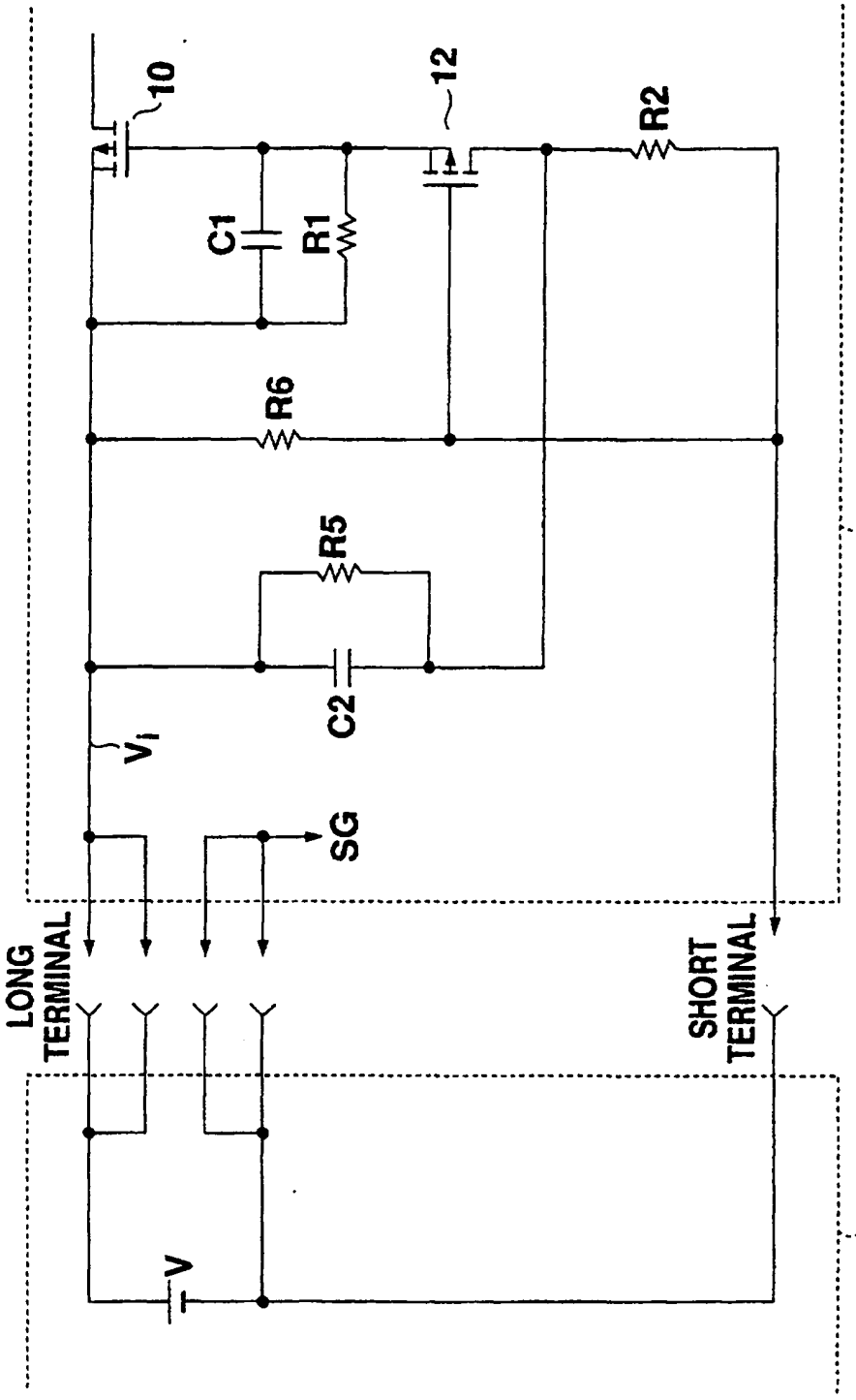
10
12
R2
C1
R1
R6
R5
C2
V_I
SG
LONG TERMINAL
SHORT TERMINAL
V
30
20

Fig. 5

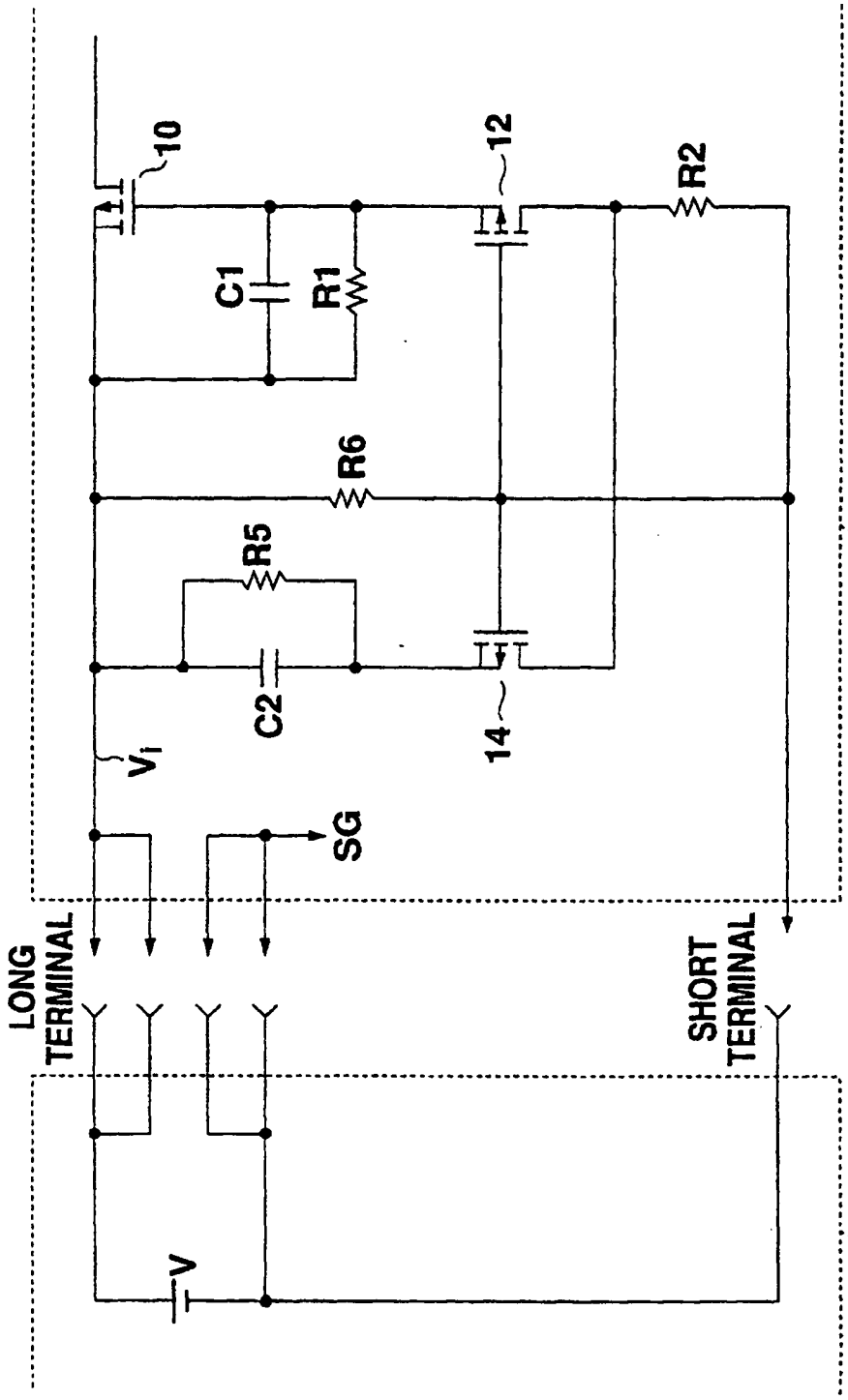
10
12
R2
C1
R1
R6
R5
C2
14
V_i
SG
LONG TERMINAL
SHORT TERMINAL
V
30
20

Fig. 6

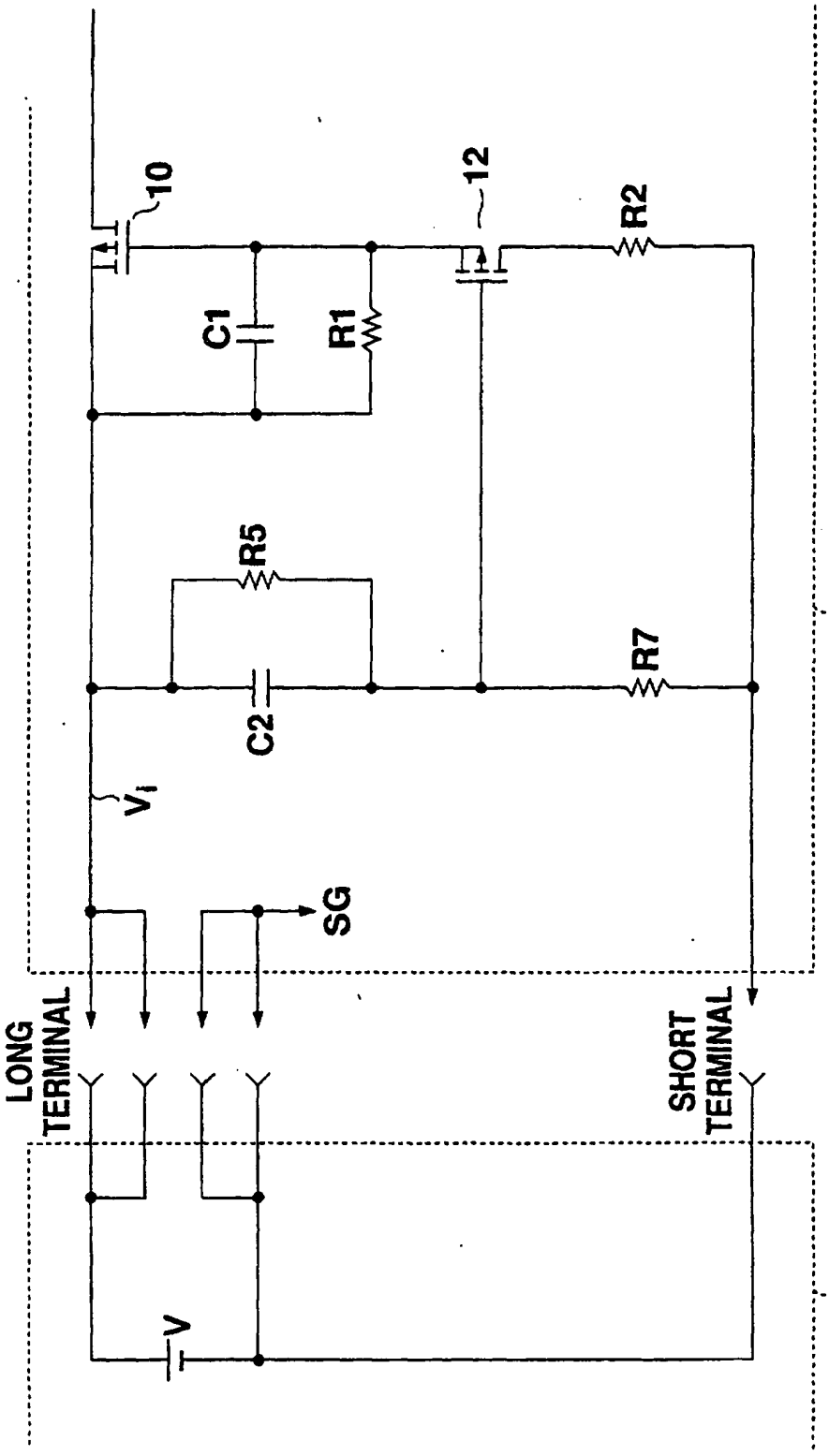
10
12
R2
C1
R1
R5
R7
C2
V_I
SG
LONG TERMINAL
SHORT TERMINAL
V
30
20

Fig. 7

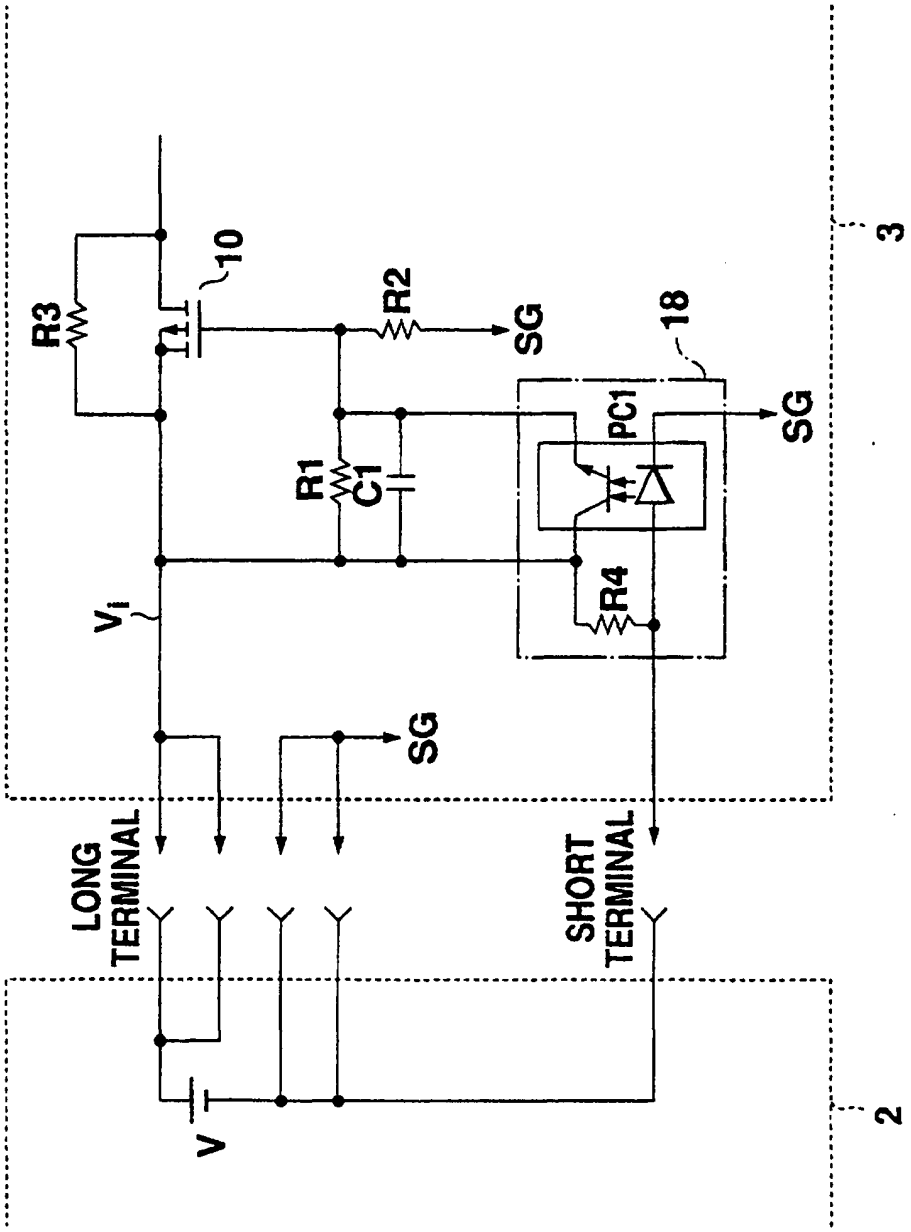
3
10
R3
R2
SG
18
PC1
SG
R1
C1
R4
V_I
SG
LONG TERMINAL
SHORT TERMINAL
V
2

Fig. 8